WHAT IS CLAIMED IS:

1. An apparatus for generating an interrupt, said interrupt being requested by an assertion of an interrupt request signal, and said apparatus comprising:

means for indicating a software condition;

means for indicating a hardware condition; and

means for generating said interrupt in response to the assertion of said interrupt request signal, said means for generating responsive to said software condition and said hardware condition.

2. An apparatus as recited in claim 1 wherein said means for generating ~~generates~~ said interrupt when said interrupt request is asserted and said hardware condition is indicated, regardless of said software condition.

3. An apparatus as recited in claim 2 wherein said means for generating comprises:

means for enabling said interrupt in response to said software condition and said hardware condition; and

means for asserting said interrupt when said interrupt request is asserted and said interrupt is enabled and for not asserting said interrupt when said interrupt request is asserted and said interrupt is not enabled.

4. An apparatus as recited in claim 1 wherein said means for indicating said software condition comprises a programmable register that outputs a software enable signal.

5. An apparatus as recited in claim 1 wherein said means for indicating said hardware condition comprises at least one hardware circuit, and wherein each of said at least one hardware circuit outputs a hardware enable signal.

6. An apparatus as recited in claim 5 wherein said means for enabling said interrupt comprises an OR gate that receives said software enable signal and said hardware enable signal and that outputs a combined enable signal.

7. An apparatus as recited in claim 27 wherein said means for asserting comprises an AND gate that receives said combined enable signal and said interrupt request signal and that outputs said interrupt.

8. An apparatus as recited in claim 7 wherein said apparatus is included in a processor, and wherein said at least one hardware circuit asserts said hardware enable signal when said processor is in a particular state.

9. An apparatus as recited in claim 8 wherein said particular state comprises an idle mode.

10. An apparatus as recited in claim 7 wherein said apparatus is included in a processor, and wherein said at least one hardware circuit asserts said hardware enable signal in response to an external enable signal generated external to said processor.

11. An apparatus as recited in claim 8 wherein said at least one hardware circuit further generates said hardware enable signal in response to an external enable signal generated external to said processor.

12. A method for generating an interrupt, said interrupt being requested by the assertion of an interrupt request signal, said method comprising the steps of:

indicating a hardware condition;

indicating a software condition; and

generating said interrupt in response to said interrupt request signal, said step of generating dependent upon said software condition and said hardware condition.

13. A method as recited in claim 12, wherein said step of generating comprises the step of generating said

interrupt when said interrupt request is asserted and said hardware condition is indicated, regardless of said software condition.

14. A method as recited in claim 13, wherein said step of generating comprises the steps of:

enabling said interrupt in response to said software condition and said hardware condition; and

asserting said interrupt when said interrupt request is asserted and said interrupt is enabled, and not asserting said interrupt when said interrupt request is asserted and said interrupt is not enabled.

15. A method as recited in claim 14, wherein said step of indicating said software condition is performed by a programmable register that outputs a software enable signal.

16. A method as recited in claim 15, wherein said step of indicating said hardware condition is performed by at least one hardware circuit, and wherein each of said at least one hardware circuit outputs a hardware enable signal.

17. A method as recited in claim 16, wherein said step of enabling said interrupt is performed by an OR gate that receives said software enable signal and said

hardware enable signal and that outputs a combined enable signal.

18. A method as recited in claim 17, wherein said step of asserting is performed by an AND gate that receives said combined enable signal and said interrupt request signal and that outputs said interrupt.

19. A method as recited in claim 18, wherein said interrupt is received by a processor, and wherein said at least one hardware circuit asserts a hardware enable signal when said processor is in a particular state.

20. A method as recited in claim 19, wherein said particular state is an idle mode.

21. A method as recited in claim 18, wherein said interrupt is received by a processor, and wherein said at least one hardware circuit asserts said hardware enable signal in response to an external enable signal generated externally of said processor.

22. A method as recited in claim 19 wherein said at least one hardware circuit further generates said hardware enable signal in response to an external enable signal generated externally of said processor.

add A3, D5